ESD5LM5.0C
ESD PROTECTION DIODE

Discription

The ESD5LM5.0C protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. Excellent clamping capability, low leakage, low capacitance, and fast response time provide best in class protection on designs that are exposed to ESD.

It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.

SOD-523

Specification Features:

- ★ Ultra Low Capacitance 2.5 pF
- ★ Low Clamping Voltage
- ★ Small Body Outline Dimensions: 0.047″ x 0.032″ (1.20 mm x 0.80 mm)
- ★ Low Body Height: 0.016″ (0.4 mm)
- ★ Stand−off Voltage: 5 V
- ★ Low Leakage
- ★ Response Time is Typically < 1.0 ns
- ★ IEC61000−4−2 Level 4 ESD Protection
- ★ This is a Pb−Free Device

Circuit Diagram

Ordering information

Product ID	Pack	Qty(PCS)
ESD5LM5.0C	SOD-523	3000

Absolute Ratings (T_{amb}=25°C)

Symbol	Parameter	Value	Units
P_{PP}	Peak Pulse Power (t_p = 8/20 μ s)	30	W
T_L	Maximum lead temperature for soldering during 10s	260	°C
T_{stg}	Storage Temperature Range	-55 to +155	°C
T_{op}	Operating Temperature Range	-40 to +125	°C
T_j	Maximum junction temperature	150	°C
	IEC61000-4-2 (ESD) air discharge contact discharge	±10 ±15	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Rating are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-5 = 1.0*0.75*0.62 in.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Device	V_{RWM} (V) Max	I_R (μA) @ V_{RWM} Max	V_{BR} (V) @ I_T (Note 2) Min	I_T mA	C (pF) Typ	V_C @ I_{PP} = 2.5 A (Note 3) Max	V_C Per IEC61000−4−2 (Note 4)
ESD5LM5.0C	5.0	1.0	5.4	1.0	2.5	12.9	Figures 1 and 2 See Below

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. Surge current waveform per Figure 5.
4. For test procedure see Figures 3 and 4.

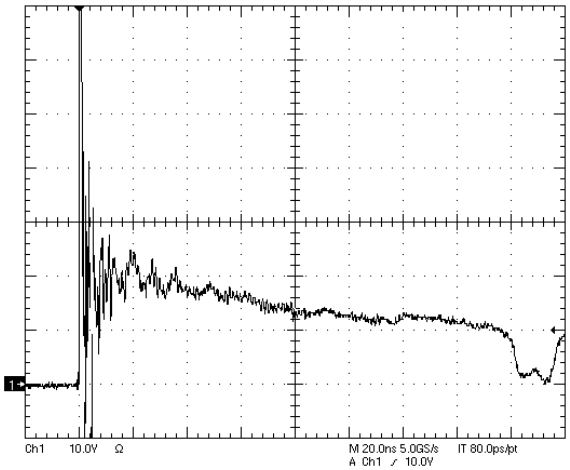


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

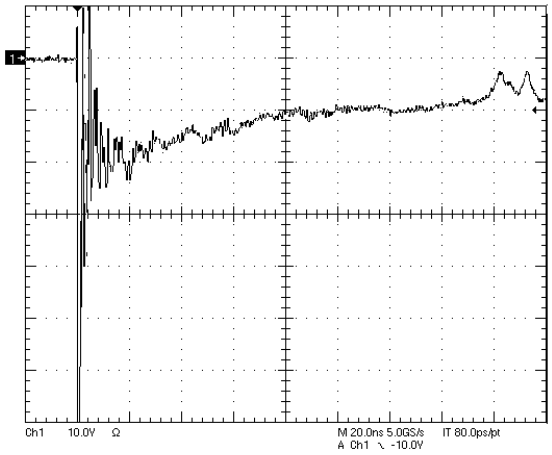


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

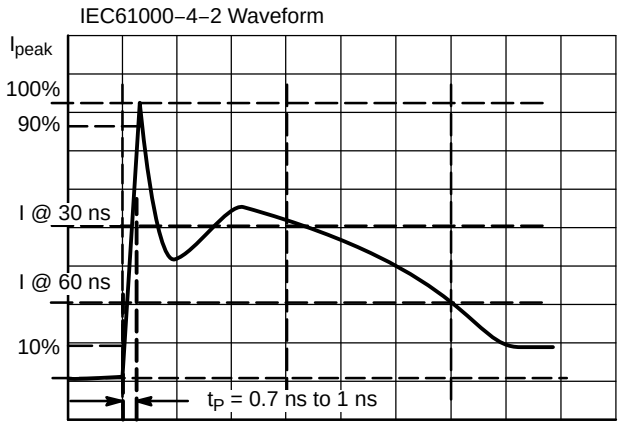
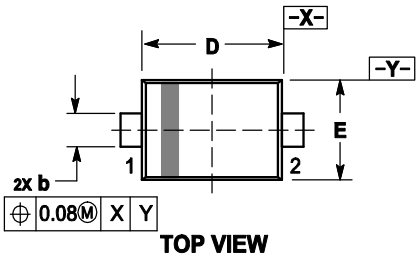
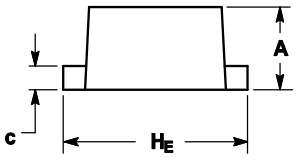


Figure 3. IEC61000−4−2 Spec

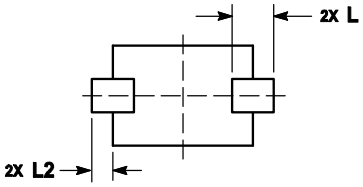
OUTLINE AND DIMENSIONS



TOP VIEW



SIDE VIEW



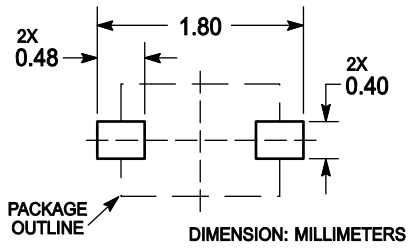
BOTTOM VIEW

Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.60	0.70	0.020	0.024	0.028
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.07	0.14	0.20	0.003	0.006	0.008
D	1.10	1.20	1.30	0.043	0.047	0.051
E	0.70	0.80	0.90	0.028	0.031	0.035
H_E	1.50	1.60	1.70	0.059	0.063	0.067
L	0.30 REF			0.012 REF		
L_2	0.15	0.20	0.25	0.006	0.008	0.010

SOLDERING FOOTPRINT



DIMENSION: MILLIMETERS